CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

forming a gate dielectric layer above a semiconducting substrate;

forming a gate electrode layer above said gate dielectric layer;

implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer; and

patterning at least said gate electrode layer to define a gate electrode comprised of a plurality of sidewalls, said sidewalls having a recess formed therein.

2. The method of claim 1, wherein forming a gate dielectric layer above a semiconducting substrate comprises forming a gate dielectric layer comprised of at least one of silicon dioxide and silicon oxynitride above a semiconducting substrate.

3. The method of claim 1, wherein forming a gate dielectric layer above a semiconducting substrate comprises thermally growing a gate dielectric layer comprised of silicon dioxide above a semiconducting substrate.

4. The method of claim 1, wherein forming a gate electrode layer above said gate dielectric layer comprises depositing a gate electrode layer above said gate dielectric layer.

5. The method of claim 1, wherein forming a gate electrode layer above said gate dielectric layer comprises forming a gate electrode layer comprised of at least one of polysilicon and amorphous silicon above said gate dielectric layer.

6. The method of claim 1, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms comprised of at least one of boron, phosphorous, arsenic, nitrogen, antimony, and indium into said gate electrode layer to define a layer of dopant material in said gate electrode layer.

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7. The method of claim 1, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer, said layer of dopant material being completely separate from said layer of dielectric material.

8. The method of claim 1, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer, said layer of dopant material defining a region of said gate electrode layer that is positioned between said layer of dopant material and said gate electrode.

9. The method of claim 1, wherein, implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer, at least a portion of said layer of dopant material being in contact with said gate dielectric layer.

10. The method of claim 1, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms at a concentration ranging from approximately $5 \times 10^{14} - 5 \times 10^{15}$ atoms/cm^2 into said gate electrode layer to define a layer of dopant material in said gate electrode layer.

11. The method of claim 1, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms at an energy level ranging from approximately 20-500 keV into said gate electrode layer to define a layer of dopant material in said gate electrode layer.

12. The method of claim 1, wherein patterning at least said gate electrode layer to define a gate electrode comprised of a plurality of sidewalls, said sidewalls having a recess formed therein, comprises etching at least said gate electrode layer to define a gate electrode comprised of a plurality of sidewalls, said sidewalls having a recess formed therein.

13. The method of claim 1, wherein patterning at least said gate electrode layer to define a gate electrode comprised of a plurality of sidewalls, said sidewalls having a recess formed therein, comprises performing an anisotropic etching process to pattern at least said gate electrode layer to define a gate electrode comprised of a plurality of sidewalls, said sidewalls having a recess formed therein.

14. A method, comprising:

thermally growing a gate dielectric layer comprised of silicon dioxide above a semiconducting substrate;

depositing a gate electrode layer comprised of polysilicon above said gate dielectric layer;

implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer; and

performing an anisotropic etching process to pattern at least said gate electrode layer to define a gate electrode comprised of a plurality of sidewalls, said sidewalls having a recess formed therein.

15. The method of claim 14, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms comprised of at least one of boron, phosphorous, arsenic, nitrogen, antimony, and indium into said gate electrode layer to define a layer of dopant material in said gate electrode layer.

16. The method of claim 14, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer, said layer of dopant material being completely separate from said layer of dielectric material.

17. The method of claim 14, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer, said layer of dopant material defining a region of said gate electrode layer that is positioned between said layer of dopant material and said gate electrode.

18. The method of claim 14, wherein, implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer, at least a portion of said layer of dopant material being in contact with said gate dielectric layer.

19. The method of claim 14, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms at a concentration ranging from approximately $5 \times 10^{14} - 5 \times 10^{15}$ atoms/cm^2 into said gate electrode layer to define a layer of dopant material in said gate electrode layer.

20. The method of claim 14, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms at an energy level ranging from approximately 20-50 keV into said gate electrode layer to define a layer of dopant material in said gate electrode layer.

21. A device, comprising:

a gate dielectric positioned above a semiconducting substrate;

a gate electrode positioned above said gate dielectric, said gate electrode comprised of a plurality of sidewalls, each of said sidewalls having a recess formed therein; and

a plurality of source/drain regions formed in said substrate.

22. The device of claim 21, wherein said gate dielectric is comprised of at least one of silicon dioxide and silicon oxynitride.

23. The device of claim 21, wherein said gate electrode is comprised of at least one of polysilicon and amorphous silicon.

24. The device of claim 21, wherein said recesses have a shape that approximately corresponds to a concentration profile of a dopant material implanted into said gate electrode.

25. The device of claim 21, wherein each of said recesses has a peak depth that ranges between approximately 100-300 Å.

26. The device of claim 21, wherein said recesses have a width that ranges from approximately 500-1000 Å.

27. The device of claim 21, wherein said gate electrode has a width, and said recesses extend along at least a portion of the width of said gate electrode.

28. A device, comprising:

a gate dielectric comprised of silicon dioxide positioned above a semiconducting substrate;

a gate electrode comprised of polysilicon positioned above said gate dielectric, said gate electrode having a width and being further comprised of a plurality of sidewalls, each of said sidewalls having a recess formed therein that extends for at least a portion of said width of said gate electrode; and

a plurality of source/drain regions formed in said substrate.

29. The device of claim 28, wherein said recesses have a shape that corresponds to a concentration profile of a dopant material implanted into said gate electrode.

30. The device of claim 28, wherein each of said recesses has a peak depth that ranges between approximately 100-300 Å.

31. The device of claim 28, wherein said recesses have a width that ranges from approximately 500-1000 Å.